Atty. Dkt. No. 035905-0104

REMARKS

1. Introduction

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons which follow. This amendment adds, changes and/or deletes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, are presented, with an appropriate defined status identifier.

Claims 1-98, 106-449, 451-455, and 467-474 are requested to be canceled. Claims 450 and 456-466 are currently being amended. Claims 483-507 are being added. Support for the amendments and the new claims may be found throughout the specification, such as on page 11, line 27, page 37, line 31, page 50, line 4 and in originally filed claims 456-482. No new matter was added.

Applicants appreciate the courtesy extended by Examiner Weiss in conducting a telephone interview with Dr. Thomas Lee, Liza Toth and the undersigned representative on June 24, 2003. In addition to the comments on the attachment to form PTO-413A, the following issues were discussed during the interview.

Page 3 of the Office Action contained an objection to the title of the invention and to claim 101. The title and claim 101 have been amended to overcome the objection.

2. Claims 99 to 105

Claims 99 to 101 have been rejected under § 103(a) as being unpatentable over Watanabe in view of Matsushita. Claims 102-105 have been rejected under § 103(a) as being unpatentable over Watanabe in view of

Matsushita and further in view of Zhang. These rejections are respectfully traversed.

As discussed during the interview, claim 99 recites that the devices are formed in an amorphous or polycrystalline semiconductor layer. Watanabe does not state that the silicon layers of the array are either amorphous or polycrystalline. Watanabe teaches that the silicon layers are formed by vapor phase epitaxial method (col. 3, line 29-34), which implies that the silicon layers could be single crystal silicon layers.

Epitaxy, from the Greek for "arrange upon," is a special process for growing films on a substrate. Its distinguishing feature is that the perfect crystalline order of the underlying substrate extends into the grown film. As epitaxial growth proceeds, the atoms align themselves according to the template represented by the substrate's crystallinity. Epitaxy's great value is that it therefore preserves monocrystallinity, while allowing, for example, the grown film to possess quite different doping levels (or even polarity) from those of the underlying substrate. Such abruptness usually cannot be achieved with standard doping techniques.

Matsushita teaches forming a three dimensional array of devices, where the device layers are single crystal silicon layers over a single crystal silicon substrate (see abstract of Matsushita). Thus, the combination of the Watanabe and Matsushita references teaches away from the claimed device where the devices are formed in an amorphous or polycrystalline semiconductor layer.

Since Watanabe does not specify the crystallinity of the silicon layers of the devices, while Matsushita teaches forming the devices in single crystal silicon layers, one of ordinary skill in the art would be motivated to form the device layers of Watanabe in single crystal silicon layers, as suggested by Matsushita. During the interview, the examiner noted that this was a reasonable argument. The examiner also indicated that Matsushita was used to provide

motivation to add a single crystal silicon substrate to the array of Watanabe. However, applicants respectfully submit that irrespective of the reasons for combining Matsushita and Watanabe, if Matsushita and Watanabe are combined, then the combination of references as a whole would teach away from the claimed amorphous or polycrystalline semiconductor layer because Matsushita teaches single crystal silicon layers.

3. Claims 456 and 458-466

Claim 456 was rejected under § 102(b) as being anticipated by or under §103(a) as being obvious over Watanabe. Claims 458 to 463 and 465 to 466 were rejected under § 103(a) as being unpatentable over Watanabe in view of Zhang. Claim 464 was rejected under § 103(a) as being unpatentable over Watanabe in view of Zhang and further in view of Kub. These rejections are respectfully traversed.

As discussed during the interview, Watanabe does not teach a planarization step for any layer of the array by any planarization method. The terms "planar member" in Watanabe refer to as-deposited conductive layers, such as word lines or bit lines (see col. 2, lines 67-68, col. 3, lines 60-61, and col. 4, lines 67-68). These conductive layers are not planarized in a planarization step.

MPEP § 2125 states that proportions or features in prior art drawings are not evidence of actual proportions unless the prior art expressly states that drawings are to scale. Just because the figures of Watanabe show straight horizontal lines does not mean that the actual layers of Watanabe are highly planar. The surfaces of the "planar members" or conductive layers of Watanabe would have a lower degree of planarity than a surface planarized by CMP because the layers of Watanabe are deposited over non-planar device features in lower levels and/or on the substrate.

Originally filed claim 456 recited that at least one surface is planarized by CMP. During the interview, the examiner indicated that claim 456 is a product claim and that the process limitation reciting that at least one surface is planarized by CMP does not provide sufficient structural limitation to this product claim. Applicants respectfully disagreed with the examiner's claim interpretation. However, in order to expedite prosecution, applicants proposed to amend claim 456 to recite amorphous or polycrystalline devices (in other words, devices which contain amorphous or polycrystalline semiconductor regions, such as channel, source or drain regions in transistor devices or p or n doped regions in diode devices) and to recite that the at least one surface was substantially planar.

Thus, claim 456 now recites a limitation similar to that of claim 99. Applicants noted during the interview that Watanabe does not specify using amorphous or polycrystalline silicon layers in the devices. The examiner indicated that he would perform a follow up search and may give claim 456 favorable consideration depending on the outcome of the search.

4. Claims 475 and 478 to 482

Claims 475 and 478 to 482 were rejected under § 103(a) as being unpatentable over Watanabe in view of Kub. Claims 476 and 477 were rejected under § 103(a) as being unpatentable over Watanabe in view of Zhang and Kub. These rejections are respectfully traversed.

As discussed during the interview, the surfaces of the "planar members" or conductive layers of Watanabe would have a lower degree of planarity than the claimed surface because the layers of Watanabe are deposited over non-planar device features in lower levels and/or on the substrate.

Kub teaches that when two wafers are bonded together, the wafer surfaces being bonded should be polished by CMP to improve wafer bonding.

Claim 475 recites a monolithic 3D array. A monolithic 3D array does not use wafer bonding to bond separately formed device levels together, as defined on page 19, lines 10-14 of the present specification:

> The term "monolithic" means that layers of each level of the array were directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device.

In other words, Kub teaches a non-monolithic 3D array because Kub teaches to separately form two dimensional arrays and then to bond or package these arrays together to form a non-monolithic 3D array. In contrast, claim 475 recites a monolithic 3D array where the layers of the array are deposited on top of each other rather than formed separately and then bonded together.[1]

There is no motivation to import the CMP method / surfaces of Kub into a monolithic 3D array, because Kub teaches that CMP improves wafer bonding, while a monolithic 3D array excludes bonded wafers. During the interview, the examiner noted that this was a reasonable argument and promised to favorably consider claim 475.

New method claims 499 to 507 contain all limitations of claim 475. Applicants respectfully request rejoinder of claims 499 to 507 upon allowance of claim 475, as provided in MPEP § 821.04.

5. Claims 103, 449, 458-461 and 477

Claim 449 has been combined with claim 450 in view of newly discovered references provided on the supplemental IDS being submitted with this Amendment.

[1] Claim 475 requires that the layers of the monolithic 3D array be deposited onto each other. However, claim 475 does not preclude bonding the monolithic 3D array to other structures, such as chip packaging or other devices, after the monolithic 3D array is completed.

Regarding claims 103, 458-461 and 477, Watanabe teaches a broad genus of devices ("any type of memory device", col. 2, lines 52-53). However, Watanabe does not teach or suggest the species of devices recited in claims 103, 458-461 and 477. In a case where the prior art teaches a broad genus, the prior art also has to provide motivation to select the claimed species from the broad genus (see MPEP § 2144.08). Watanabe provides no such motivation.

For example, as discussed during the interview Watanabe does not teach or suggest making rail stack TFT EEPROMs as recited in claim 461, a preferred embodiment of which is described on pages 74-97 of the present application. Similarly, Watanabe does not teach or suggest making pillar devices as recited in claims 458 and 459, various embodiments of which are described on pages 22-49 of the present application. Nor does Watanabe does teach or suggest making self-aligned TFT EEPROMs as recited in claim 460, various embodiments of which are described on pages 49-73 of the present application. The examiner disagreed, stating that Watanabe disclosed any type of EEPROM devices. However, if such a broad teaching in Watanabe is sufficient to render all EEPROM structures obvious, then no other applicant would have been able to obtain a patent claiming a new EEPROM structure after the Watanabe patent issued.

6. IDS

The examiner requested that PTO forms SB08 that were previously filed but not initialed be attached to the present Amendment. Applicants respectfully requested that the examiner initial and return with the next Office Action the attached forms SB08 that were previously submitted with IDS's filed 11/27/01 and 6/11/02, but not acknowledged in the Office Action mailed June 3, 2003.

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7. Conclusion

Applicants believe that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested. The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

Date 7/15/03

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The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.